WHAT IS CLAIMED IS:

1. An apparatus comprising:

an integrated circuit comprising a first logic path and a second logic path;

a first transistor having a first gate length and a first gate centerline-to-contact spacing, the first transistor positioned on the first logic path; and

a second transistor having a second gate length that is greater than the first gate length and a second gate centerline-to-contact spacing that is substantially equal to the first gate centerline-to-contact spacing, the second transistor positioned on the second logic path.

2. The apparatus of Claim 1, wherein the second logic path comprises a path delay that is less than a critical path delay of the integrated circuit.

3. The apparatus of Claim 1, wherein the integrated circuit is an application specific integrated circuit.

4. The apparatus of Claim 1, wherein the difference between the first gate length and the second gate length is smaller than a length of a grid of a design rule for the integrated circuit.

5. The apparatus of Claim 1, wherein the integrated circuit comprises one or more power grids, each of the one or more power grids having a uniform power grid spacing, and wherein the first transistor and the second transistor are in the one or more power grids.

6. The apparatus of Claim 1, wherein the first logic path is a critical path.

7. A method for designing an integrated circuit, comprising:

providing a first transistor in a first logic path, the first transistor having a first contact, a first gate length and a first contact to gate centerline spacing;

providing a second transistor in a second logic path, the second transistor having a second contact, a second gate length and a second contact to gate centerline spacing, the first contact to gate centerline spacing substantially equal to the second contact to gate centerline spacing; and

selecting a different gate length for the first gate length using a predetermined design criterion.

8. The method of Claim 7, wherein the first gate length and the second gate length are equal, and selecting a different gate length comprises selecting a different gate length without changing the placement of the first contact or the second contact.

9. The method of Claim 8, wherein providing a first transistor comprises providing a first cell comprising the first transistor and wherein selecting a different gate length comprises replacing the first cell with a substitute cell comprising a substitute transistor, the substitute transistor having a different gate length than the first gate length, the first cell and the substitute cell having the same footprint and operable to perform a same function.

10. The method of Claim 7, wherein the predetermined design criterion is based on the respective levels of leakage current of the first transistor and the second transistor.

11. The method of Claim 7, wherein the first logic path is a critical path and the different gate length is a gate length that is shorter than the first gate length.

12. The method of Claim 7, wherein the first logic path is a non-critical path and the different gate length is a gate length that is longer than the first gate length.

13. The method of Claim 7, wherein modeling a change of the gate length comprises changing the gate length by a length increment, the length increment less than the length of one grid of a design rule for the integrated circuit.

14. A system, comprising:

a computer system having a display unit, an input device, and a processor;

a computer readable medium coupled to the computer system, the computer readable medium comprising a program operable, when executed on the processor, to:

generate a plurality of cell models, each of the cell models modeling at least one transistor disposed on a logic path of an integrated circuit, the at least one transistor having a gate and a contact, the gate comprising a gate length and a centerline, the distance between the centerline of the gate and the contact modeled by the each of the cell models substantially equal for all of the plurality of cell models;

identify at least one of the plurality of cell models using a predetermined criterion; and

for each identified cell model, model a change of the gate length without modeling a movement of any contact.

15. The system of Claim 14, wherein the logic path is a critical path and the program is operable to model a change of the gate length by modeling a shorter gate length.

16. The system of Claim 14, wherein the logic path is on a non-critical path and the program is operable to model a change of the gate length by modeling a longer gate length.

17. The system of Claim 14, wherein the logic path is a critical path and the program is operable to model a change of the gate length by substituting the each identified cell model with a substitute cell model, the substitute cell model modeling at least one substitute transistor having a shorter gate length than the gate length modeled by the each identified cell model, wherein the each identified cell model and the corresponding substitute cell model are operable to perform a same logic function.

18. The system of Claim 14, wherein the logic path is a non-critical path and the program is operable to model a change of the gate length by substituting the each identified cell model with a substitute cell model, the substitute cell model modeling at least one substitute transistor having a longer gate length than the gate length modeled by the each identified cell model, wherein the each identified cell model and the corresponding substitute cell model are operable to perform a same logic function.

19. The system of Claim 14, wherein the predetermined criterion is based on the respective levels of leakage current of a plurality of cells, the plurality

of cells modeled by the corresponding plurality of cell models.

20. The system of Claim 14, and further comprising a means for manufacturing the integrated circuit, the means coupled to the computer system, and wherein the program is further operable to direct the means to manufacture the integrated circuit according to a final model generated by the computer system after modeling the change of the gate length.